

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of operating a computer having a pipelined processor, comprising setting a bit within an instruction text field of a branch, said bit preventing the branch from being placed into a branch history buffer and into a branch target buffer to thereby prevent the branch from being written into the branch history buffer and branch target buffer and predicted and to make the branch only detectable at the time frame of decode.
2. (Previously Amended) The method as defined in claim 1 comprising predicting the direction and target of a branch prior to decode.
3. (Previously Amended) The method as defined in claim 2 comprising predicting the direction and target of a branch prior to decode through a branch prediction array.
4. (Previously Amended) The method as defined in claim 1 comprising tracking the branch from the beginning of the pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array.
5. (Previously Amended) The method as defined in claim 1 comprising denoting the instruction text field as a non-writable branch into the BTB.
6. (Previously Amended) The method as defined in claim 5 comprising denoting the instruction text field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked from being written to the BTB.

7. (Previously Amended) The method as defined in claim 6 comprising predicting; the branch via aliasing.

8. (Previously Amended) The method as defined in claim 1 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer.

9. (Canceled)

10. (Previously Amended) The method as defined in claim 8 comprising denoting state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area.

11. (Currently Amended) A computer system having input, output, storage, and a pipelined processor, said processor adapted and configured to set a bit within an instruction text field of a branch, said bit preventing the branch from being placed into a branch history table and a branch target buffer to thereby prevent the branch from being written into the branch history buffer and branch target buffer and predicted and make the branch only detectable at the time frame of decode.

12. (Previously Amended) The computer system as defined in claim 11, said computer system adapted and configured to predict the direction and target of a branch prior to decode.

13. (Previously Amended) The computer system as defined in claim 12 said computer system adapted and configured to predict the direction and target of a branch prior to decode through a branch prediction array.

14. (Previously Amended) The computer system as defined in claim 11, said computer system adapted and configured to track the branch from the beginning of the pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array.

15. (Previously Amended) The computer system as defined in claim 11 said computer system adapted and configured to denote the instruction text field as a non-writable branch into the BTB.

16. (Previously Amended) The computer system as defined in claim 15 said computer system adapted and configured to denote the instruction text field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked from being written to the BTB.

17. (Previously Amended) The computer system as defined in claim 16 said computer system adapted and configured to denote the instruction text field in the non-system area, and to predict the branch via aliasing.

18. (Previously Amended) The computer system as defined in claim 11 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer.

19. (Canceled)

20. (Previously Amended) The computer system as defined in claim 18 said computer system is adapted and configured to denote state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area is prevented.

21. (Currently Amended) A program product comprising a storage medium having computer readable program code, said program code for use in a computer system having

input, output, storage, and a pipelined processor, said program code adapting and configuring the computer system to set a bit within an instruction text field of a branch, said bit preventing the branch from being placed into a branch history table and a branch target buffer to thereby prevent the branch from being written into the branch history buffer and branch target buffer and predicted and make the branch only detectable at the time frame of decode.

22. (Previously Amended) The program product as defined in claim 21, said computer system adapted and configured to predict the direction and target of a branch prior to decode.

23. (Previously Amended) The program product as defined in claim 22 said computer system adapted and configured to predict the direction and target of a branch prior to decode through a branch prediction array.

24. (Previously Amended) The program product as defined in claim 21, said computer system adapted and configured to track the branch from the beginning of the pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array.

25. (Previously Amended) The program product as defined in claim 21 said computer system adapted and configured to denote the instruction text field as a non-writable branch into the BTB.

26. (Previously Amended) The program product as defined in claim 25 said computer system adapted and configured to denote the instruction text field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked from being written to the BTB.

27. (Previously Amended) The program product as defined in claim 26 said computer system adapted and configured to denote the instruction text field in the non-system area, and predict the branch via aliasing.

28. (Previously Amended) The program product as defined in claim 21 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer.

29. (Canceled)

30. (Previously Amended) The program product as defined in claim 28 said computer system is adapted and configured to denote state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area.